# MANO'S BASIC COMPUTER

BY TEAM: على الله

# Team members

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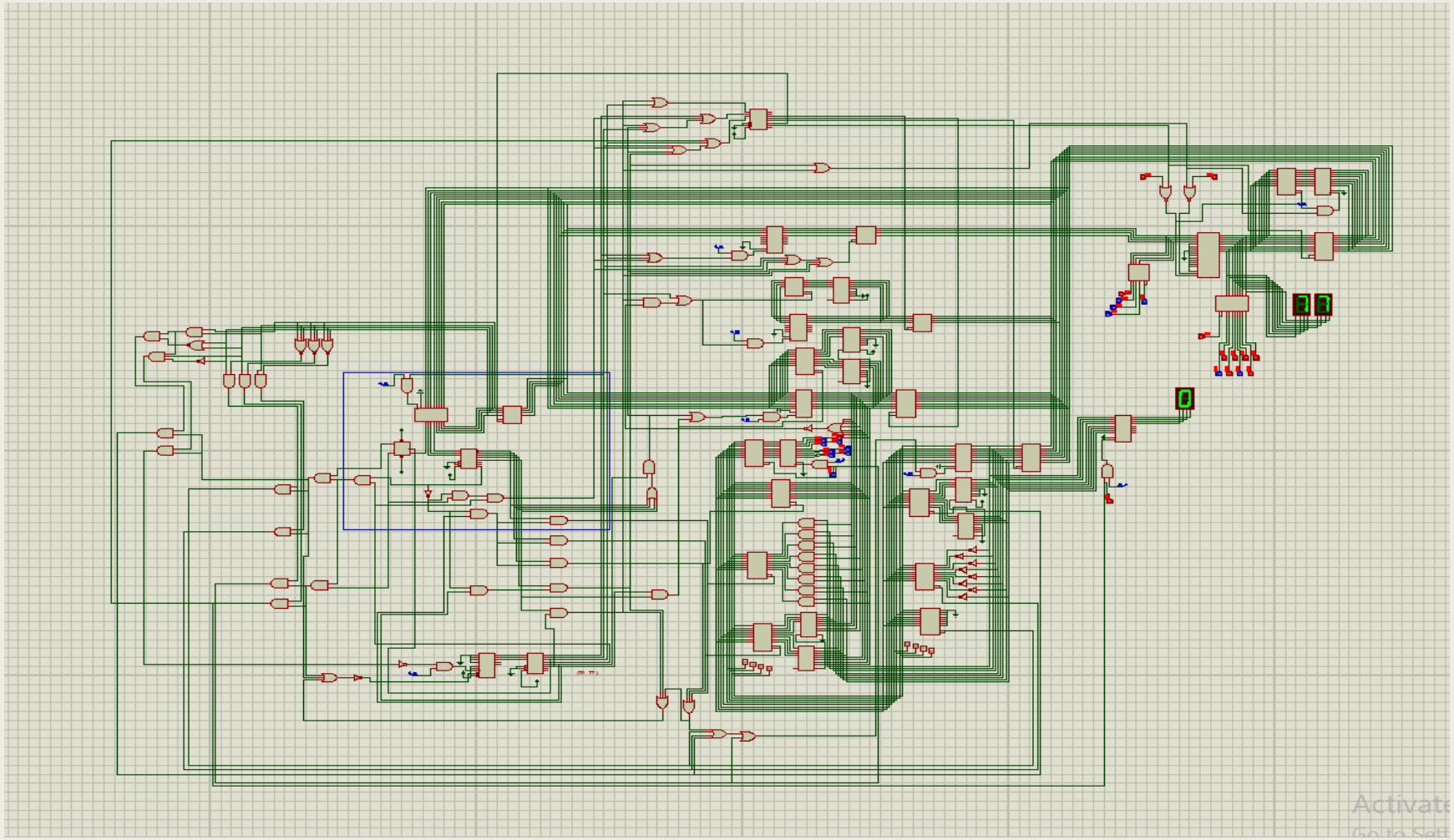
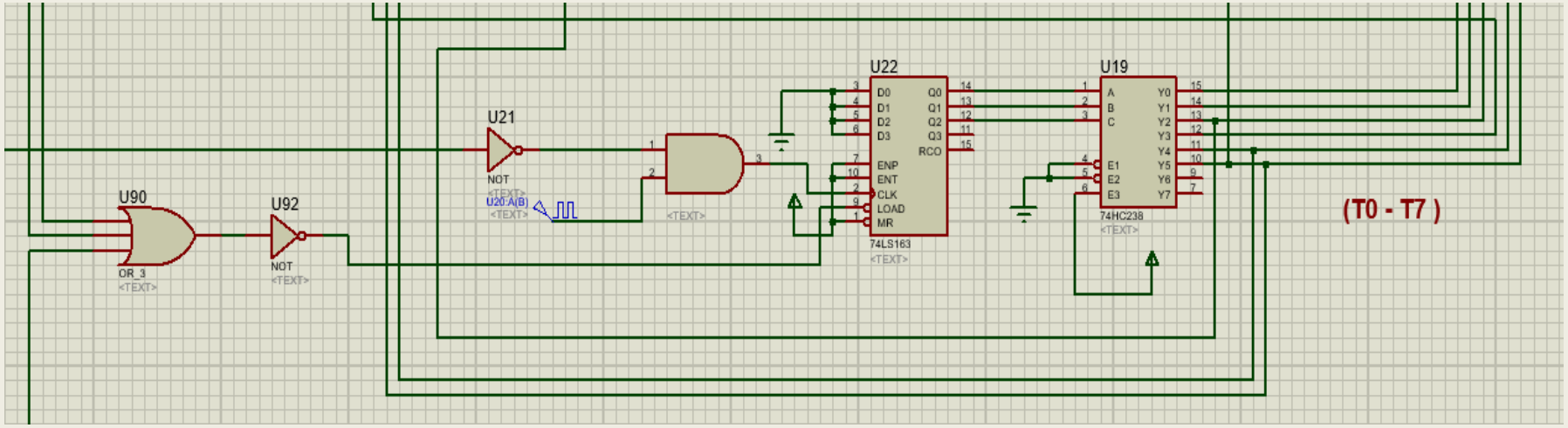
# Mano’s Computer



# Parts of Mano's Computer

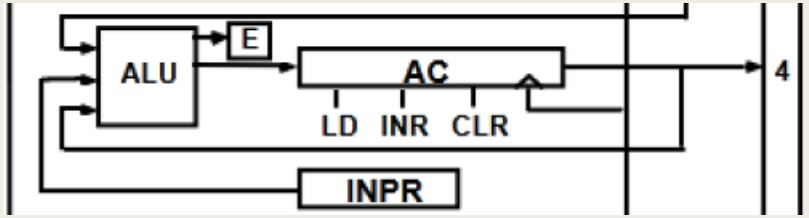
1- SC

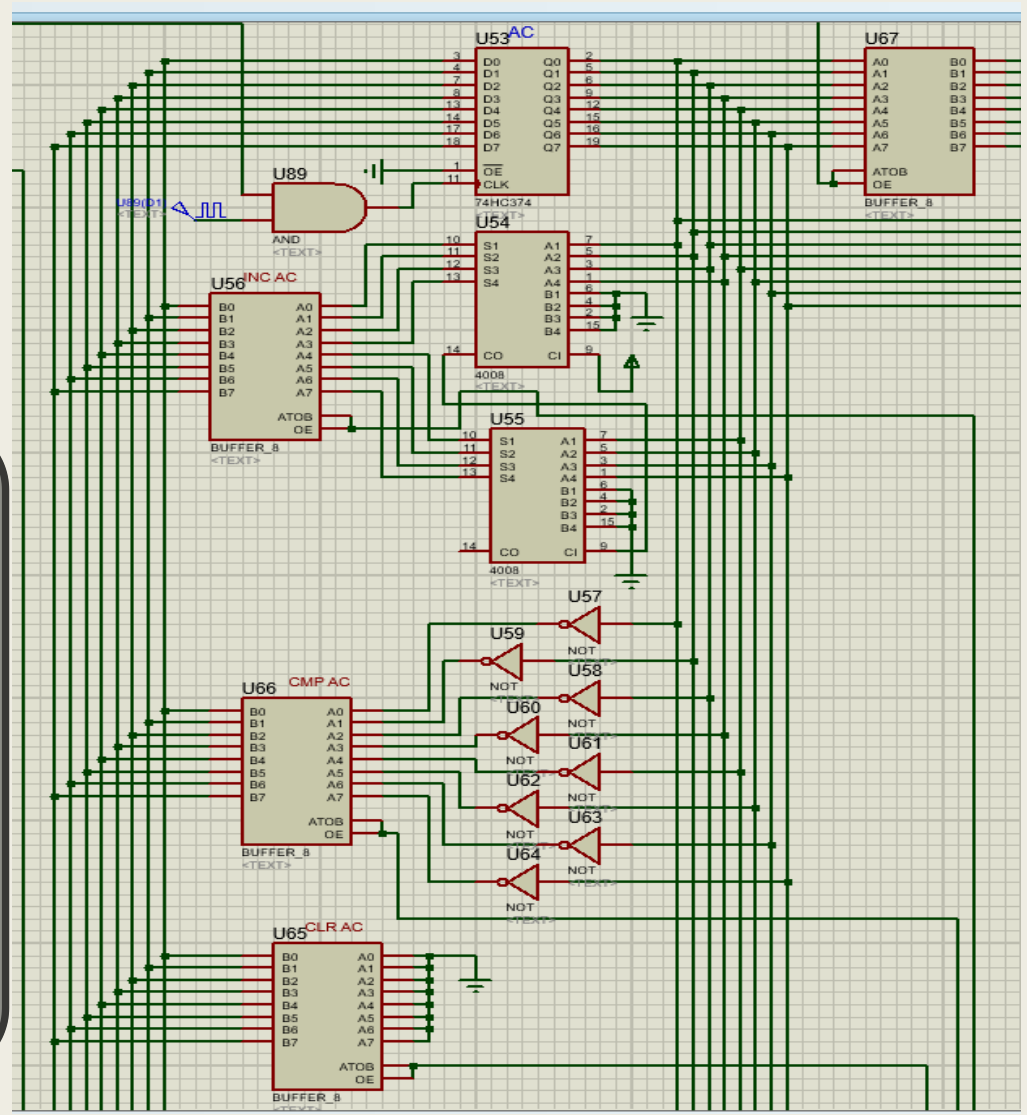
يعد تصميم بمثابة عداد للزمن من (T0 – T7)



# Parts of Mano's Computer

2- AC




بتتم ثلاث عمليات عليه

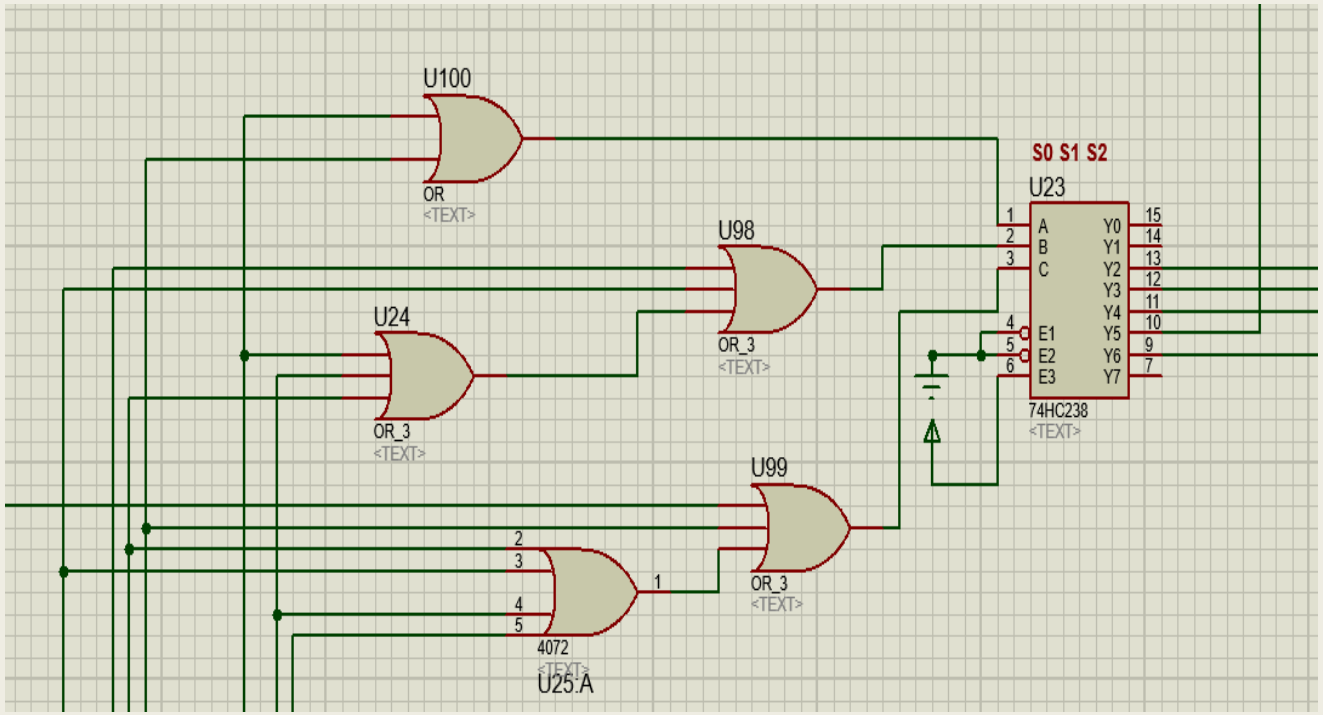
CLR
بوصل Buffer
بدخل كله اصفار

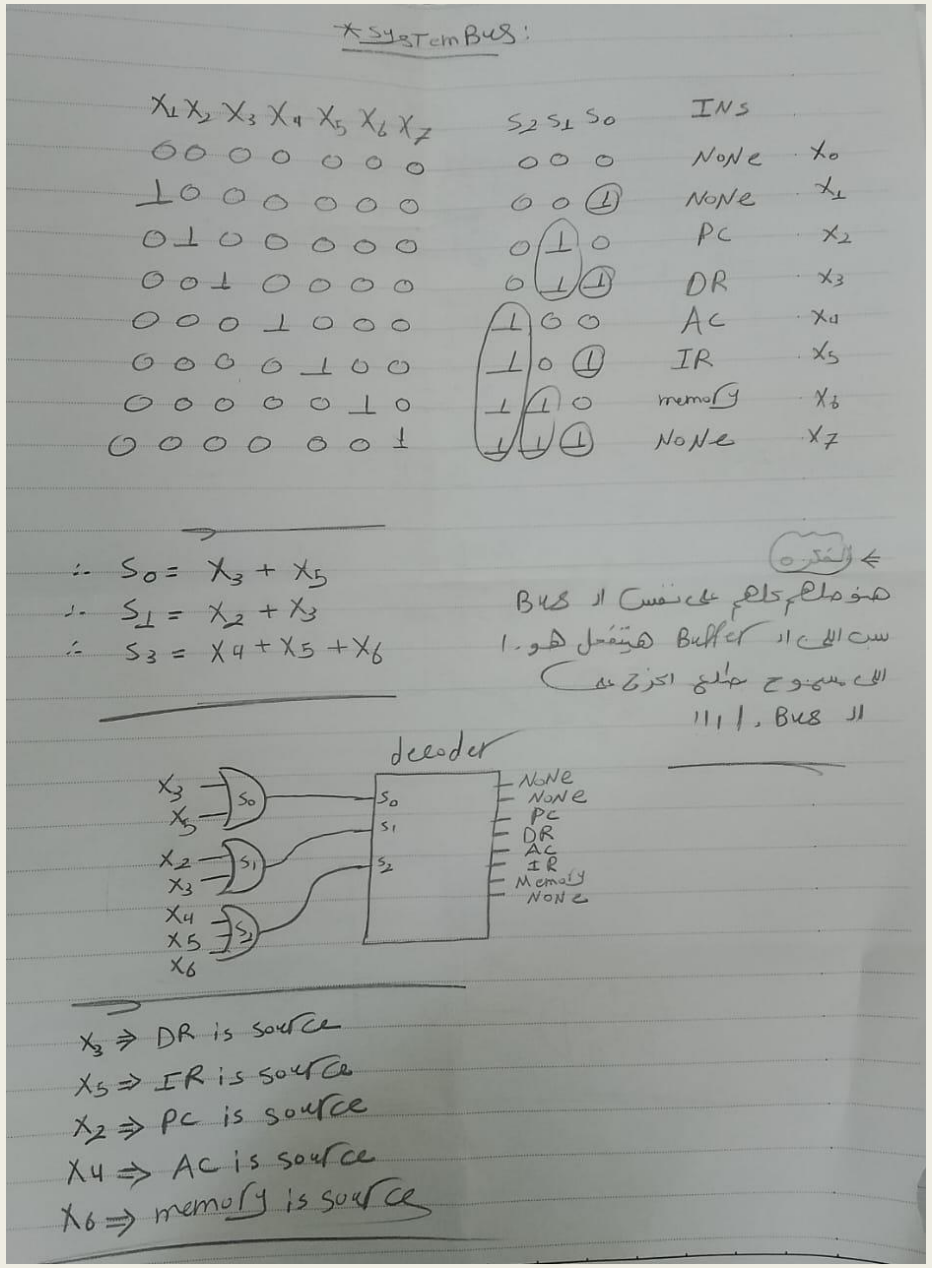
CMP
بدخل الدخل
على دوائر NOT

INC
بضيف واحد من
خلال ADDER
على محتوى ال
AC

# Parts of Mano's Computer

## 3- System Bus



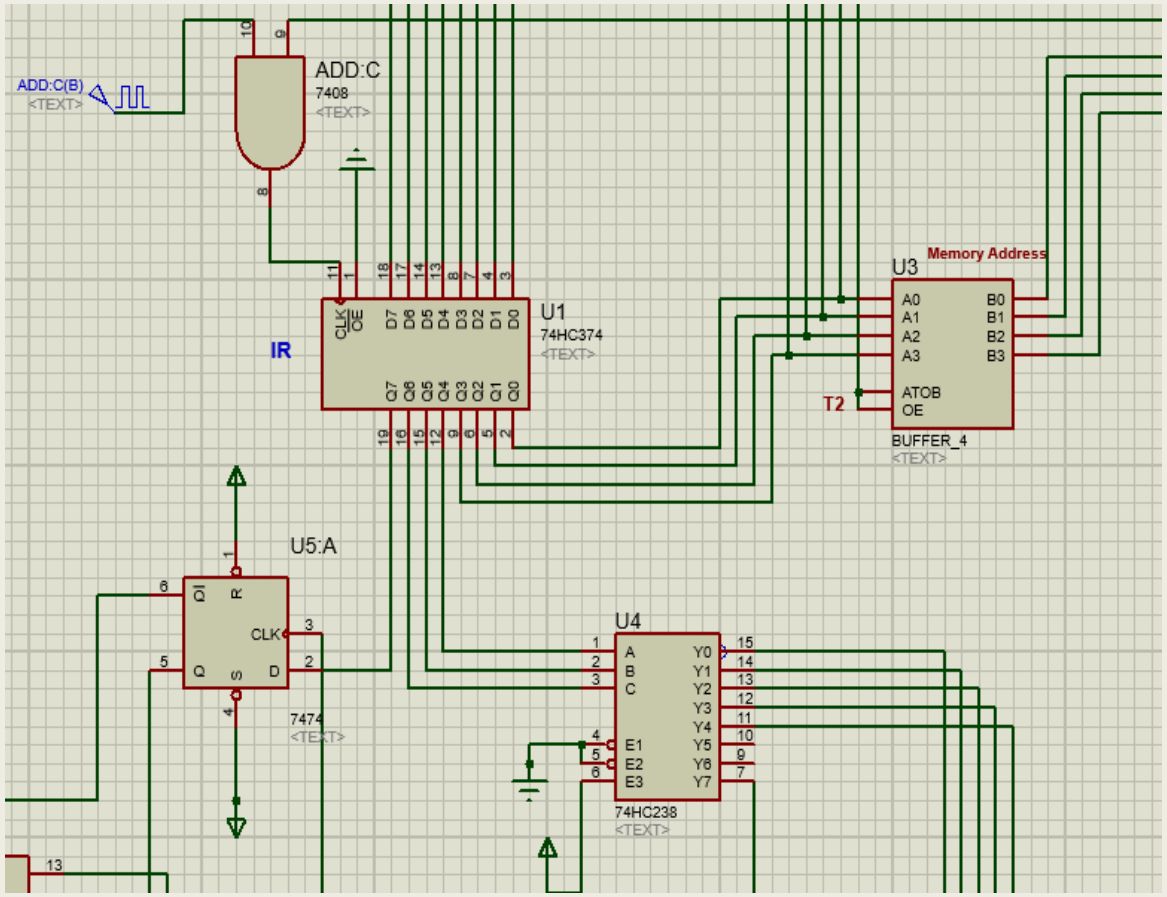
# Parts of Mano's Computer

## 4- IR

بناخد اول اربعه Bit و ندخلهم Adress
لل Memory

بناخد ثانى ثلاث Bits و ندخلهم على
ديكودر ٣*٨

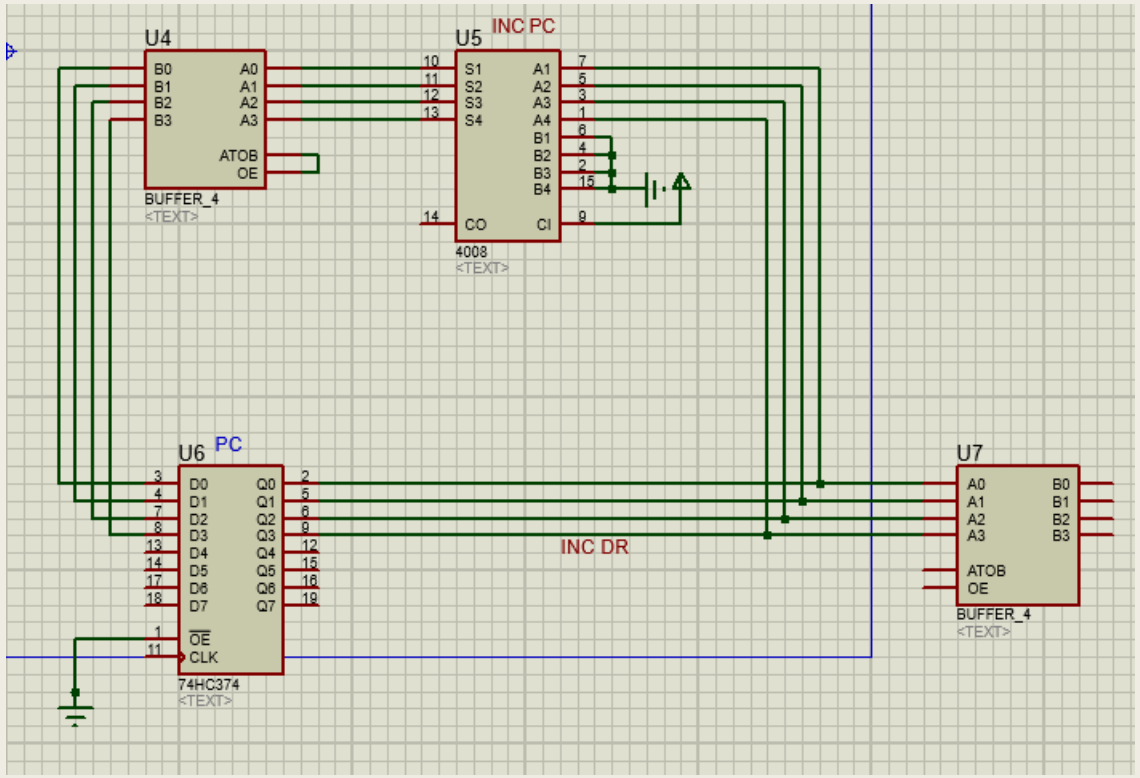
بالنسبة لاخر Bit تسمى I و هي
مهمه في Timing and control



# Parts of Mano's Computer

## 5- PC

وظيفته انه بينقل محتواه الى ال AR
وبعدها يتم زيادة محتواة بمقدار واحد



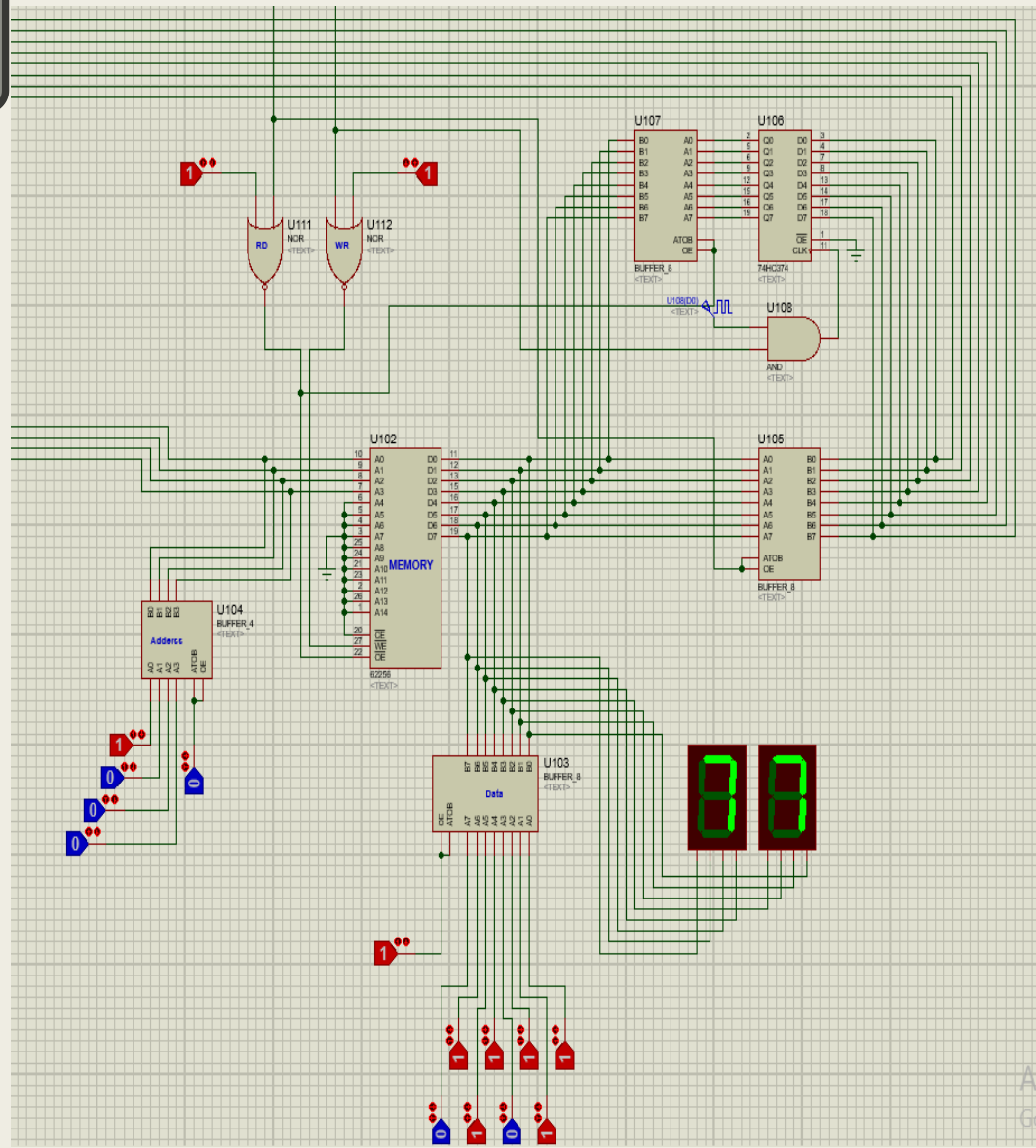
# Parts of Mano's Computer

## 6- Memory

يتم تسجيل محتوى الميموري
من خلال تفعيل خانة ال Write

يتم تحديد ال Adress المراد
تخزين فيه Operand

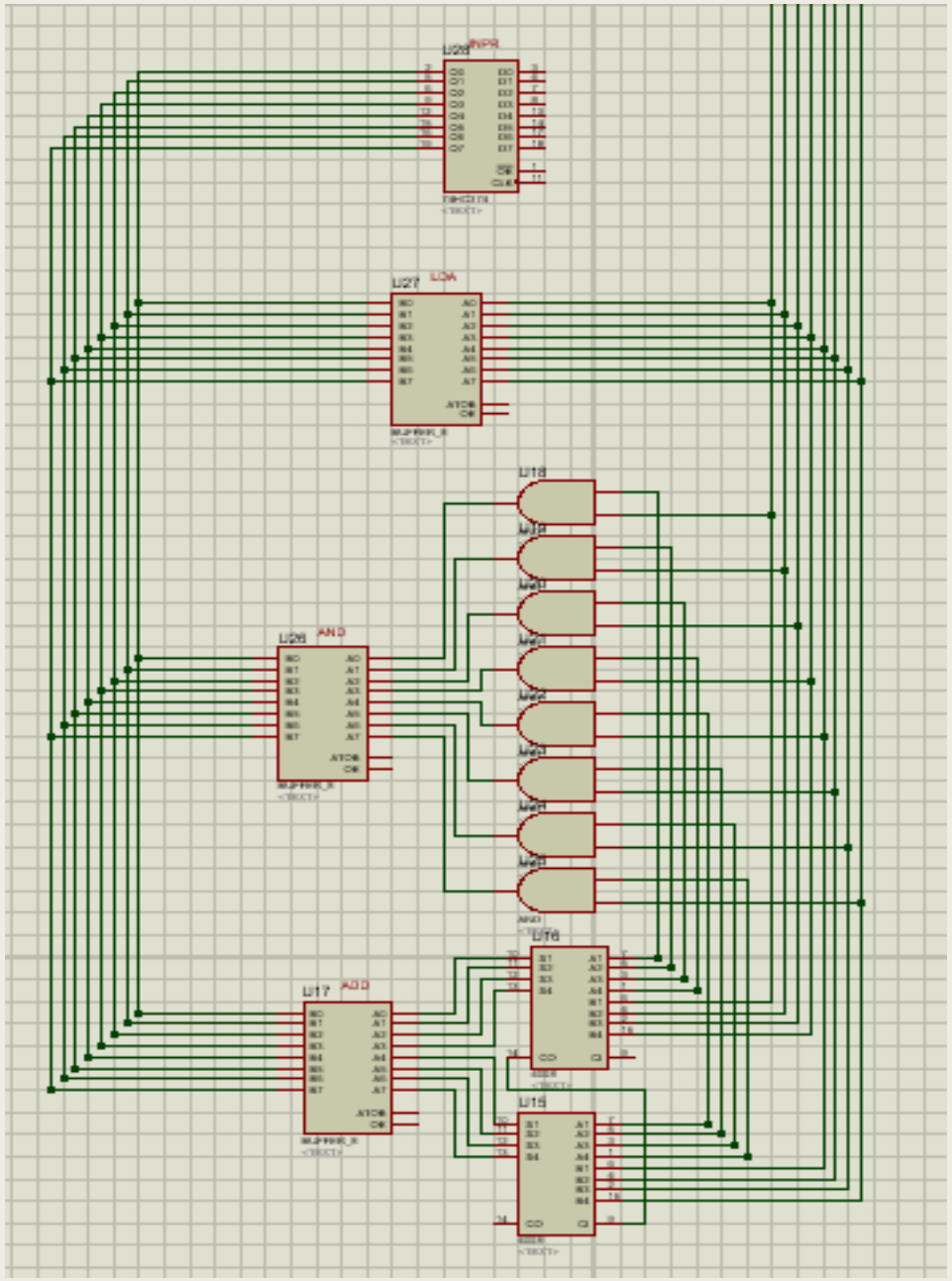
يتم تفعيل خانة الRead و
ادخال Adress فيظهر الناتج
على الخرج



# Parts of Mano's Computer

## 7- ALU

هي الوحدة المسئولة عن
عمليات ال AND & ADD & LDA



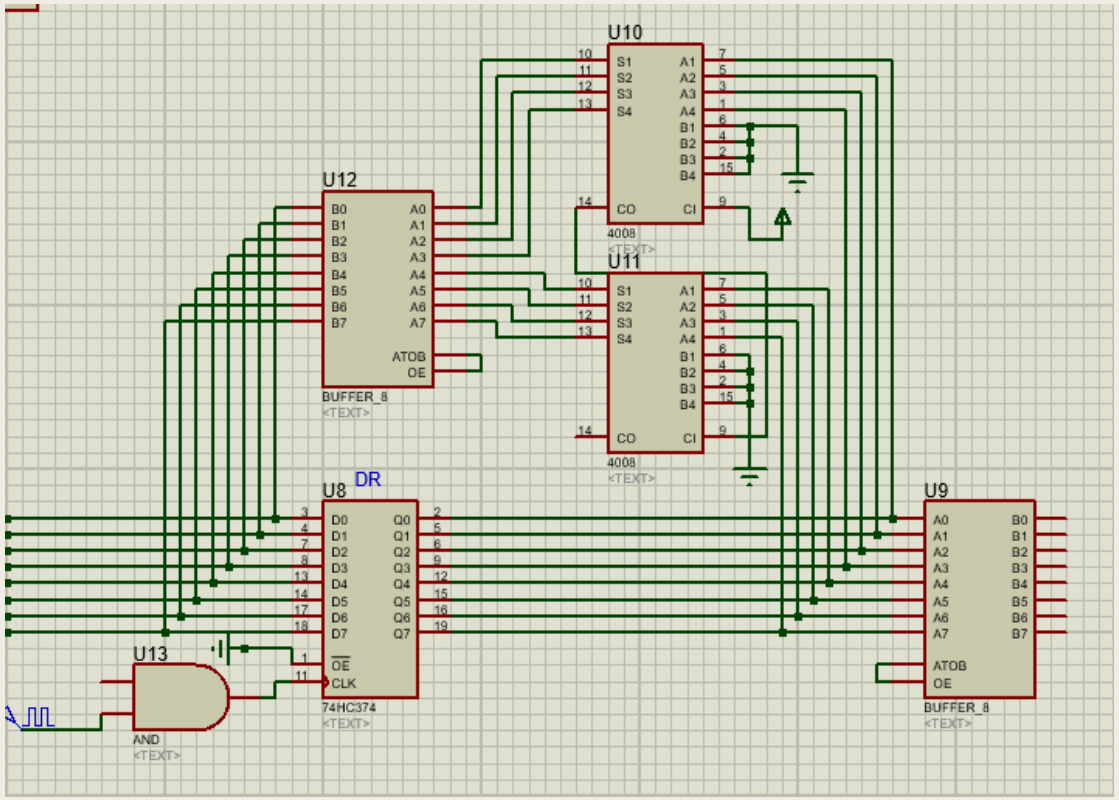
# Parts of Mano's Computer

## 8- DR

هو الطرف الثاني لعمليات Memory reference

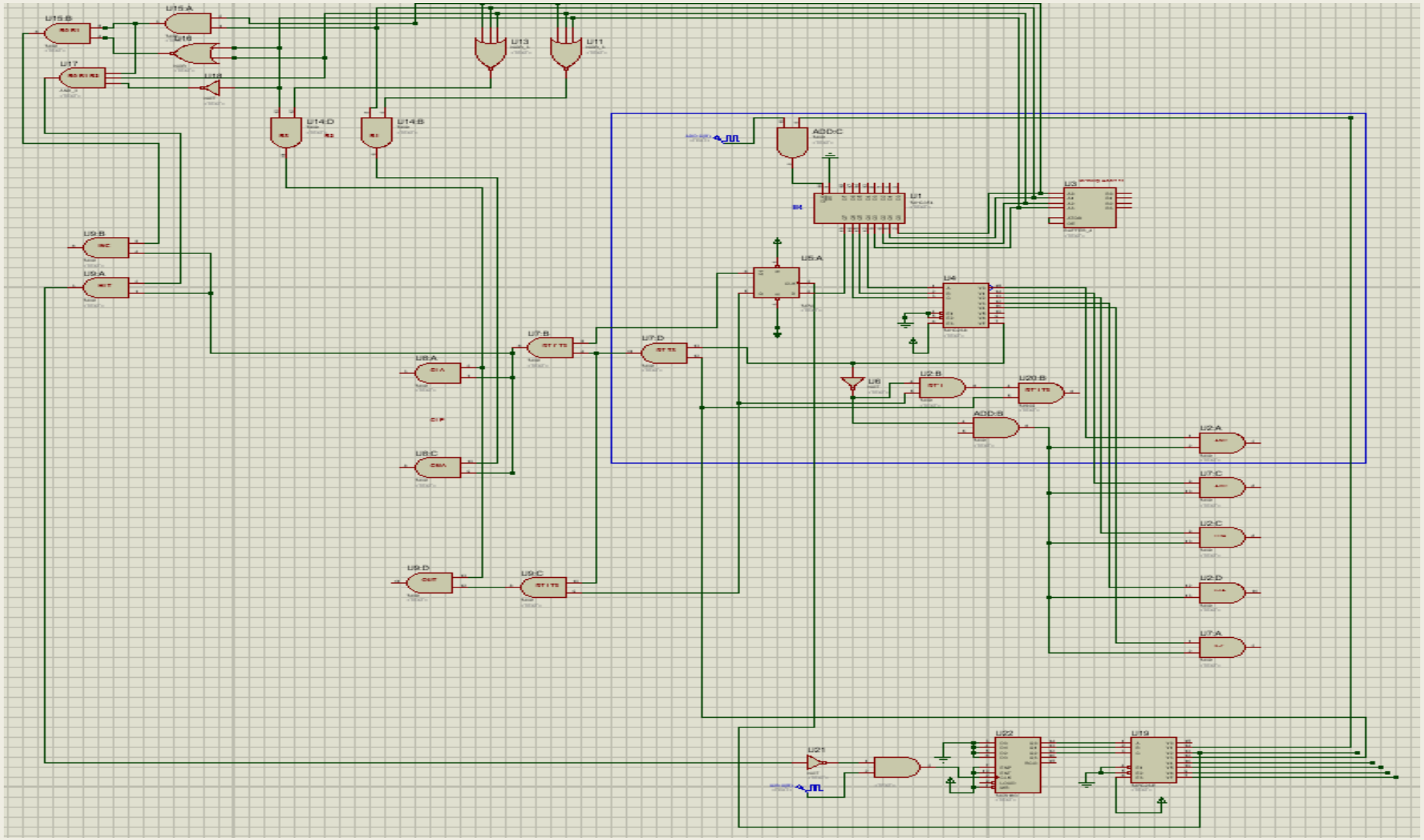
كما هو واضح تم عمل دائرة INC لتنفيذ عملية ISZ

ISZ هو زيادة محتوى الميمورى بمقدار واحد



# Parts of Mano's Computer

## 9- Timing & Control



# What does the project implement?

| Memory Reference | Register Reference | In/Out put Reference |
| --- | --- | --- |
| 0X → AND | 78 → CLR | F8 → IN |
| 1X → ADD | 72 → CMP | F4 → OUT |
| 2X → LDA | 73 → INC | |
| 3X → STA | 77 → HLT | |
| 4X → ISZ | | |

# Control functions and Micro operation for the Basic computer

| | | |
|---|---|---|
| Fetch | $R'T_0$ : | $AR \leftarrow PC$ |
| | $R'T_1$ : | $IR \leftarrow M[AR]$ , $PC \leftarrow PC + 1$ |
| Decode | $R'T_2$ : | $D_0, \ldots\ldots D_7 \leftarrow$ Decode IR(12-14), |
| | | $AR \leftarrow IR(0\text{-}11)$, $I \leftarrow IR(15)$ |
| Indirect | $D'_7IT_3$ : | $AR \leftarrow M[AR]$ |

## → Memory – reference:

| | | |
|---|---|---|
| AND | $D_0T_4$ : | $DR \leftarrow M[AR]$ |
| | $D_0T_5$ : | $AC \leftarrow AC \wedge DR$ , $SC \leftarrow 0$ |
| ADD | $D_1T_4$ : | $DR \leftarrow M[AR]$ |
| | $D_1T_5$ : | $AC \leftarrow AC + DR$ , $E \leftarrow C_{OU1}$, $SC \leftarrow 0$ |
| LDA | $D_2T_4$ : | $AC \leftarrow M[AR]$ |
| | $D_2T_5$ : | $AC \leftarrow DR$, $SC \leftarrow 0$ |
| STA | $D_3T_4$ : | $M[AR] \leftarrow AC$, $SC \leftarrow 0$ |
| ISZ | $D_6T_4$ : | $DR \leftarrow M[AR]$ |
| | $D_6T_5$ : | $DR \leftarrow DR + 1$ |
| | $D_6T_6$ : | $M[AR] \leftarrow DR$, if $(DR = 0)$ then $(PC \leftarrow PC + 1)$ , $SC \leftarrow 0$ |

## → Register – reference :

$D_7I'T_3 = r$ ( common to all register – reference instructions )

$IR(i) = B_i$ ( $i = 0, 1, 2, 3, 4, \ldots\ldots, 11$ )

| | | |
|---|---|---|
| CLA | $rB_{11}$ : | $AC \leftarrow 0$ |
| CMA | $rB_9$ : | $AC \leftarrow AC$ |
| INC | $rB_5$ : | $AC \leftarrow AC + 1$ |
| HILT | $rB_0$ : | $S \leftarrow 0$ |

## → Output / Input – reference :

$D_7IT_3 = p$ ( Common to all input / output instruction )

$IR(i) = R_i$ ( $i = 6, 7, 8, 9, 10, 11$ )

| | | |
|---|---|---|
| INP | $pB_{11}$ : | $AC(0-7) \leftarrow INPR$ |
| OUT | $pB_{10}$ : | $OUTR \leftarrow AC(0-7)$ |

# THANKS